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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/562,295	12/22/2005	Patrice Gamand	FR03 0067 US	3265

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
09/23/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/562,295	GAMAND, PATRICE	
	Examiner	Art Unit	
	JUNGHWA M. IM	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 7 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Mastromatteo (US 6653655).

Regarding claim 1, Fig 1 of Mastromatteo shows a microelectronic chip assembly comprising:

at least three microelectronic chips (4, 5, 6) that are stacked together, at least one of the chips, denoted intermediate chip (5), comprising via holes (22) filled with conductive material running through said chip, characterized in that said intermediate chip is realized from a high-ohmic substrate (col. 2, lines 32-55) comprising

devices to be used by at least two other microelectronic chips (4, 6), called top and bottom chips, are arranged on at least one face of said intermediate chip, said top and bottom chips being connected by flip chip bonding on top and bottom faces of said intermediate chip, respectively, said via holes (22) realizing an electrical connection between pads of said top and bottom chips.

Regarding claim 7, Fig 1 of Mastromatteo shows said intermediate chip comprises integrated devices on both sides.

Regarding claim 8, Fig 1 of Mastromatteo shows at least three devices that are integrated on separate chips, characterized in that said chips are arranged in an assembly.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mastromatteo in view of Shieh et al. (US Pub. 2003/0160316), hereinafter Shieh.

Regarding claim 2, Fig 1 of Mastromatteo shows most aspects of the instant invention except “said intermediate chip, which is also linked by flip chip bonding to an extern al connection device, makes the connection with external circuits possible." Fig. 1 of Shieh shows an intermediate chip (2) linked by flip chip bonding to an extern al connection device (1), makes the connection with external circuits possible. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Shieh into the device of Mastromatteo in order to have an intermediate chip

linked by flip chip bonding to an extern al connection device with external circuits for operating functionally.

Regarding claim 3, Fig. 3 of Shieh shows high and low-performance sensitive devices are integrated on said bottom, intermediate and top chips in order that said devices are stacked in a specific order relative to said connection device, said specific order being such that high- performance sensitive devices are integrated on the bottom chip and low-performance sensitive devices are integrated on the top chip.

Regarding claim 9, Fig 1 of Mastromatteo shows a device formed by a method of manufacturing a miniaturized packaged system including at least a microelectronic assembly (1), characterized in that said method includes the steps of:

realizing at least one chip from a high-ohmic substrate (5), called intermediate chip, including integrated devices on at least one face and via holes (22) running through said chip and filled with conductive material (col. 2, line 32 - col. 23, line 32),

linking at least one chip, called bottom chip (4), including integrated devices on one face, by bonding on said intermediate chip, in order that said via holes are connected with terminal pads of said bottom chip, linking the intermediate chip by flip bonding on a connection device in order that said bottom chip is stacked between said intermediate chip and said connection device,

linking by flip chip bonding a third chip (6), called top chip, including integrated devices on one face, on said intermediate chip, in order that said via holes are in connection with terminal pads of said top chip.

Fig 1 of Mastromatteo shows most aspects of the instant invention except "linking the intermediate chip by flip chip bonding on a connection device in order that said bottom chip is stacked between said intermediate chip and said connection device," and "molding the assembly in a molding component." Fig. 1 of Shieh shows an intermediate chip (2) linked by flip chip bonding to an extern al connection device (1), making the connection with external circuits possible and molding the assembly in a molding component (5). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Shieh into the device of Mastromatteo in order to have an intermediate chip linked by flip chip bonding to an extern al connection device with external circuits for operating functionally and molding the assembly in a molding component for protection of the device.

Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mastromatteo in view of Shieh as applied to claim 2 above, and further in view of Ichitsubo et al. (US 6633005), hereinafter Ichitsubo.

Regarding claims 4-6, the combination of Mastromatteo/Shieh shows most aspects of the instant invention except that a high-frequency device is integrated on said bottom chip, said bottom chip being in contact with a heat sink (a heat dissipative device) is integrated on said bottom chip. Fig. 4 of Ichitsubo shows a

high-frequency device (24; RF IC) is integrated on said bottom chip, said bottom chip being in contact with a heat sink (26) is integrated on said bottom chip. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Ichitsubo into the device of Mastromatteo/Shieh in order to have a high-frequency device integrated on the bottom chip for RF application and the bottom chip being in contact with a heat sink for heat dissipation to the air.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JUNGHWA M. IM whose telephone number is (571)272-1655. The examiner can normally be reached on MON.-FRI. 7:30AM-4:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Junghwa M. Im/
Examiner, Art Unit 2811

/J. M. I./
Examiner, Art Unit 2811